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# Computation of SRT and CORDIC Division Algorithms

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***Abstract :****With increasing on chip complexities the on chip area is a major concern. Today users desire every gadget to be small enough, particularly the hand held systems. The design of a fast divider is an important issue in high-speed computing .Many of the DSP applications try to closely simulate real time images. Speed, clarity and resemblance to real time objects are some of the issues to be addressed to achieve this goal. Trigonometric function calculation is one of the primary tasks performed in DSP applications. The paper presents a fast radix-2 SRT division algorithm and CORDIC division algorithm. In SRT division ,an estimated quotient digit is first calculated, instead of finding the correct quotient digit . CORDIC (Coordinate Rotation Digital Computer) is an iterative algorithm which is used to calculate mathematical functions such as trigonometric, hyperbolic, exponential functions and so on. This method reduces the computation to addition subtractions compares and shifts. SRT and CORDIC division algorithms are implemented using Xilinx ISE 10.1 simulator. The power, area and delay of the algorithms are computed using cadence.*
***Keywords -****cadence.CORDIC,Fastdivider,SRT,Xilinx.*

## I. INTRODUCTION

Performing division requires making a choice of quotient digits starting with the most significant,and progressing to the least significant digits. A simple and widely implemented class of division algorithm is digit recurrence. The most common implementation of digit recurrence division in modern microprocessors is *SRT* division, taking its name from the initials of Sweeney, Robertson and Tocher, who developed the algorithm independently at approximately the same time. SRT division uses subtraction as the fundamental operator to retire a fixed number of quotient in each iteration. Various techniques have been proposed for increasing division performance, including cascading simple low-radix stages, overlapping sections of one stage with another stage, and prescaling the input operands . All of these methods introduce area-performance tradeoffs.The main concept of this algorithm is based on the very simple and long lasting fundamentals of two dimensional geometry. The CORDIC algorithm mainly has two working modes, the rotation mode and the vectoring mode. The algorithm can be used to generate sine and cosine signals when it works in the former mode. In this paper, we only focus on the rotation angle ratherthan the vector magnitude, so the problem of SF compensation is elegantly avoided. We pursue a novel CORDIC structure design with the minimum number of iterations but without loss of accuracy. The concept of rotation is describes a circular movementwith respect to a point.

## II. SRT DIVISION ALGORITHM

To perform fast division, we would like an algorithm which has a low latency (in cycles) and a short cycle time. The latency is set by the radix r; higher radix offer lower latencies. The cycle time is set by the operations occurring in each cycle: quotient digit selection and partial remainder generation. The simplest form of division, like that taught in elementary school, uses non-redundant quotient digits and partial remainder representations. This technique requires the quotient selection logic to exactly compare the partial remainder and divisor using a slow n-bit subtraction. An n-bit subtraction is also required to find the next partial remainder.

The key idea of SRT division is to guess the quotient digit based on a few of the most significantdivisor and partial remainder bits, rather than computing it exactly. As long as the guess is close enough, the algorithm can correct on subsequent steps using redundant quotient digits.

Theoretically Steps involved in SRT algorithm

Step1:Considering radix r , where

$p_j$ is partial remainder

$q_j$ quotient digit
a = r/2
k = ar/(r-1)

Step2: SRT algorithm states that

$p_{j+1} = r(p_j - q_j * divisor)$

Step3: partial remainder is chosen such a way that it should satisfy, $|p_j| \leq k$

Step4: Choose quotient digits($q_j$) such that it should satisfy,

$| p_j - q_j * divisor | \leq k/r * divisor$

Step5: Computation is carried out until zero remainder is obtained

Step6: Quotient bit is obtained in each iteration

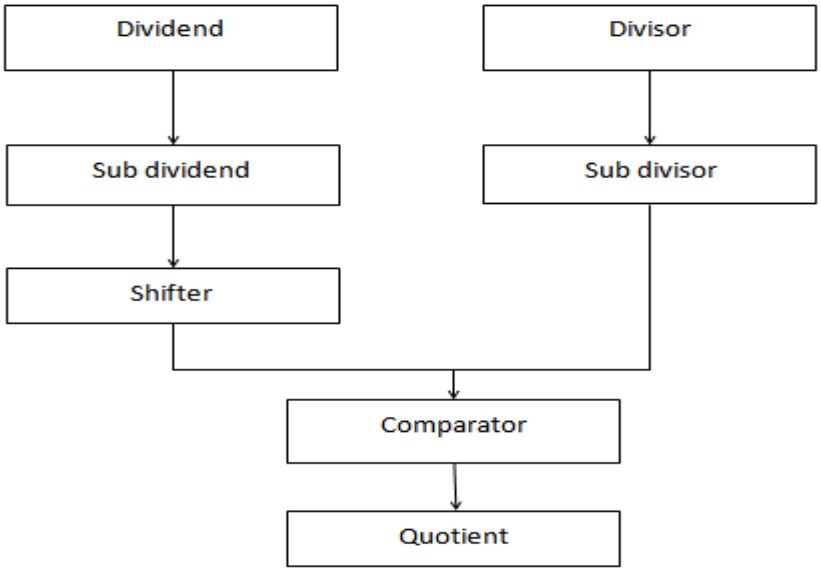


**Fig.1** Flow Diagram of SRT Algorithm

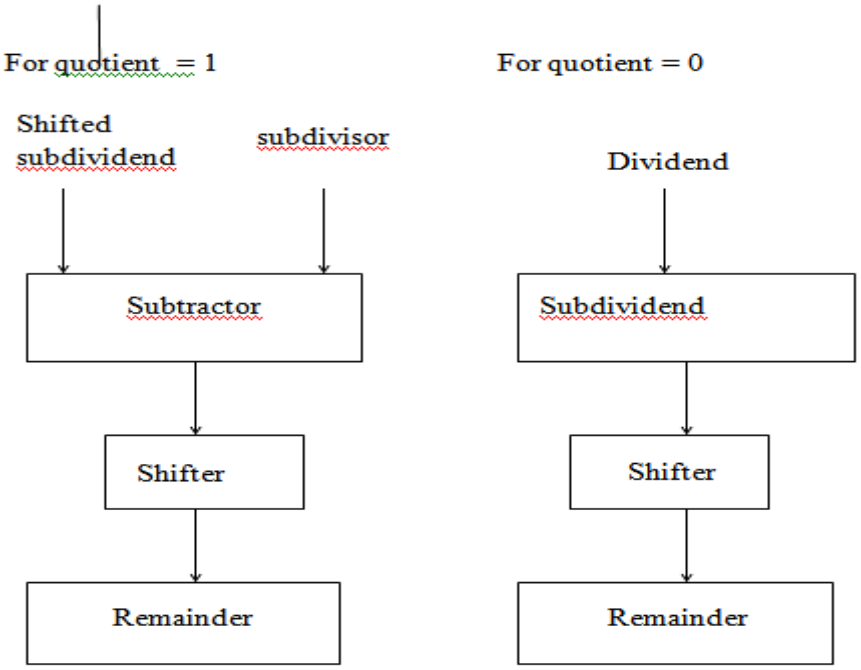


**Fig.2** Flow Diagram SRT Division Algorithm

**a. SRT Simulation Results**

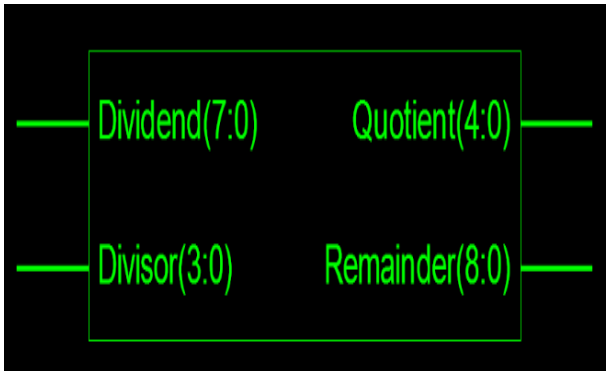


**Fig.3**RTL Schematic of SRT

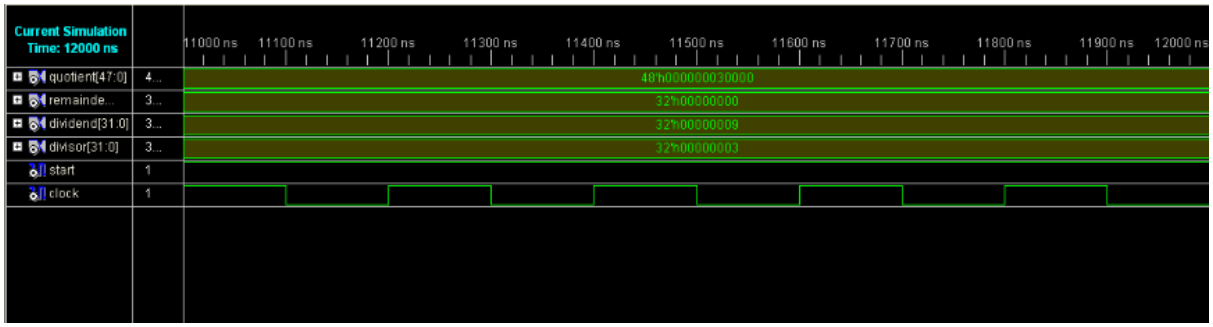


**Fig.4** Simulation Result

## III. CORDIC DIVISION ALGORITHM

CORDIC is an iterative algorithm capable of calculating trigonometric and various other functions. In this algorithm with the help of an adder/subtractor, a small look up table and a shifter the trigonometric functions can be calculated very easily. The advantage that CORDIC offers over other algorithms are that it does not require multiplication or division blocks, instead it works only with a shifter, adder/subtractor and a small lookup table.

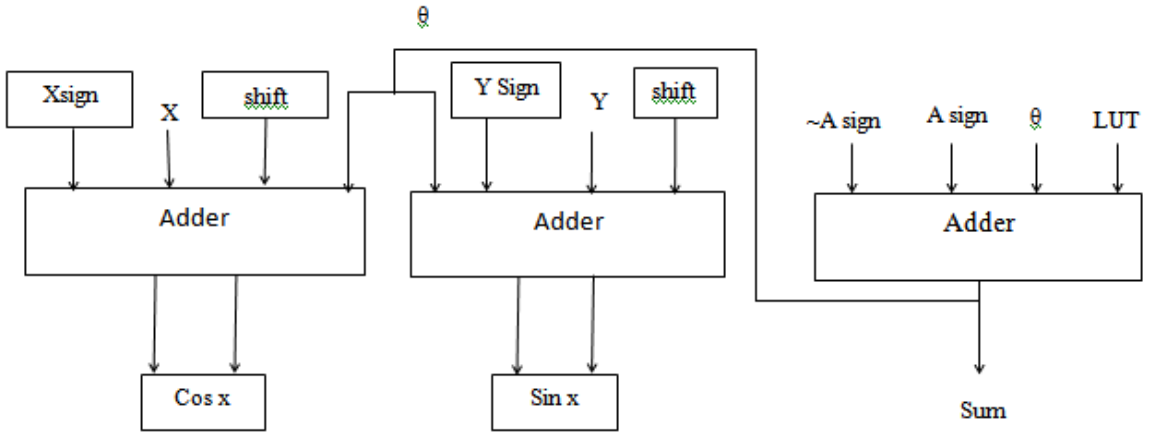


**Fig.5**Flow Diagram of CORDIC Algorithm

**a. CORDIC Simulation Results**

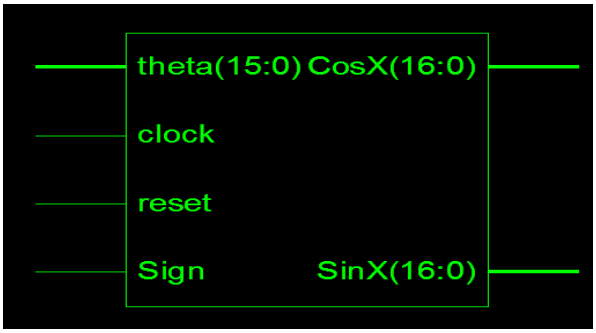


**Fig.6** RTL Schematic of CORDIC

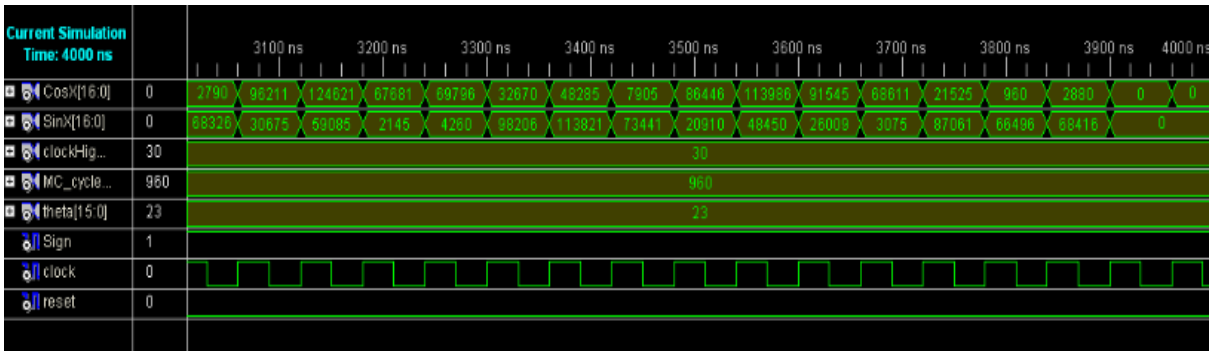


**Fig.7**Simulation Result

## III.Performances Result of The Two Division Algorithm

Division algorithms are implemented using Xilinx software and power ,delay and area are computed using cadence tool

**Table.1 cadence Results**

| Division Algorithms | Gates | Power (W) | Area |
|---|---|---|---|
| SRT | 3545.94 | 0.0008421 | 3546 |
| CORDIC | 721 | 0.000727 | 721 |

## IV.CONCLUSION

The proposed division method first speculates a quotient digit. The speculated digit is used to compute the two possible partial remainders, for the next step, in parallel with the quotient-digit correction process. The CORDIC algorithm has been successfully simulated for calculating the Sine and Cosine of an angle is represented on 10.1ISE simulator using the Verilog HDL programming language.

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